DS26303
OCTAL 3.3V T1/E1/J1 SHORT HAUL LIU
PRODUCT BRIEF

www.maxim-ic.com

FEATURES

- Eight complete E1, T1, or J1 short haul LIUs
- Independent E1 or T1 or J1 selections for each of the LIU's in non-hardware mode
- Internal software-selectable transmit and receive-side termination for 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 120 Ω E1 twisted pair and 75 Ω E1 coaxial applications
- Crystal-less jitter attenuator that can be selected for transmit or receive paths. The jitter attenuator meets ETSI CTR 12/13, ITU G.736, G.742, G.823 and AT&T PUB 6411
- Selectable single rail and dual rail mode and AMI or HDB3/ B8ZS line encoding and decoding
- Detection and generation of AIS as per G.775, ETSI 300233 for E1 and T1.231 for T1
- Digital/analog loss of signal detection as per T1.231, G.775 and ETSI 300233
- G.772 non-intrusive port monitoring
- Built in BERT for diagnostics
- Transmit open and short circuit detection
- Receiver sensitivity to -15 dB
- 8-bit parallel interface support for Intel or Motorola modes.
- 4-wire selectable serial interface
- Hardware mode for operation without a microprocessor
- Specification compliance to the latest T1 standards --- ANSI T1.102, AT&T Pub 62411, T1.403 and T1.408
- Specification compliance to the latest E1 Standards -- ITU G.703, G.742, G.775, G.823 and ETS 300 233

APPLICATIONS

- PABX and ISDN PRI
- SONET/SDH and PDH Multiplexer
- LAN/WAN Routers
- WIRELESS BASE STATION
- CSU/DSUs

ORDERING INFORMATION

PBGA Package			
DS26303N-XXX	160 pin	PBGA	–40°C to +85°C
DS26303-XXX	160 pin	PBGA	0°C to +70°C
LQFP Package			
DS26303LN-XXX	144 pin	LQFP	–40°C to +85°C
DS26303L-XXX	144 pin	LQFP	0°C to +70°C
Note: In E1 mode the device defaults to 75 ohm impedance when XXX is 075 and 120 ohm impedance when it is 120.			

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STANDARDS COMPLIANCE

ANSI T1.102	Digital Hierarchy Electrical Interface.
ANSI T1.107-1995	Digital Hierarchy – Formats Specification
ANSI T1.231-1997	Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring
ANSI T1.403	Network and Customer Installation Interface- DS1 Electrical Interface
ANSI T1.404-1994	Network-to-Customer Installation – DS3 Metallic Interface Specification
ITUT G.703	Physical/Electrical Characteristics of G.703 Hierarchical Digital Interfaces
ITUT G.736	Characteristics of Synchronous Digital Multiplex Equipment operating at 2048 Kbit/s
ITUT G.742	Second Order Digital Multiplex Equipment Operating at 8448 Kbit/s
ITUT G.775-1993	Protected Monitoring Points Provided on Digital Transmission Systems
ITUT G.775	Loss of Signal (LOS) and Alarm Indicator Signal (AIS) Defect Detection And Clearance Criteria
ITUT G.823	The control of jitter and wander within digital networks which are based on 2.048 Kbit/s Hierarchy
ETSI 300 233- May 1994	Integrated Service Digital Network (ISDN) Access Digital Section for ISDN Primary Rate

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Figure 1.1-1 DS26303 Functional Block Diagram

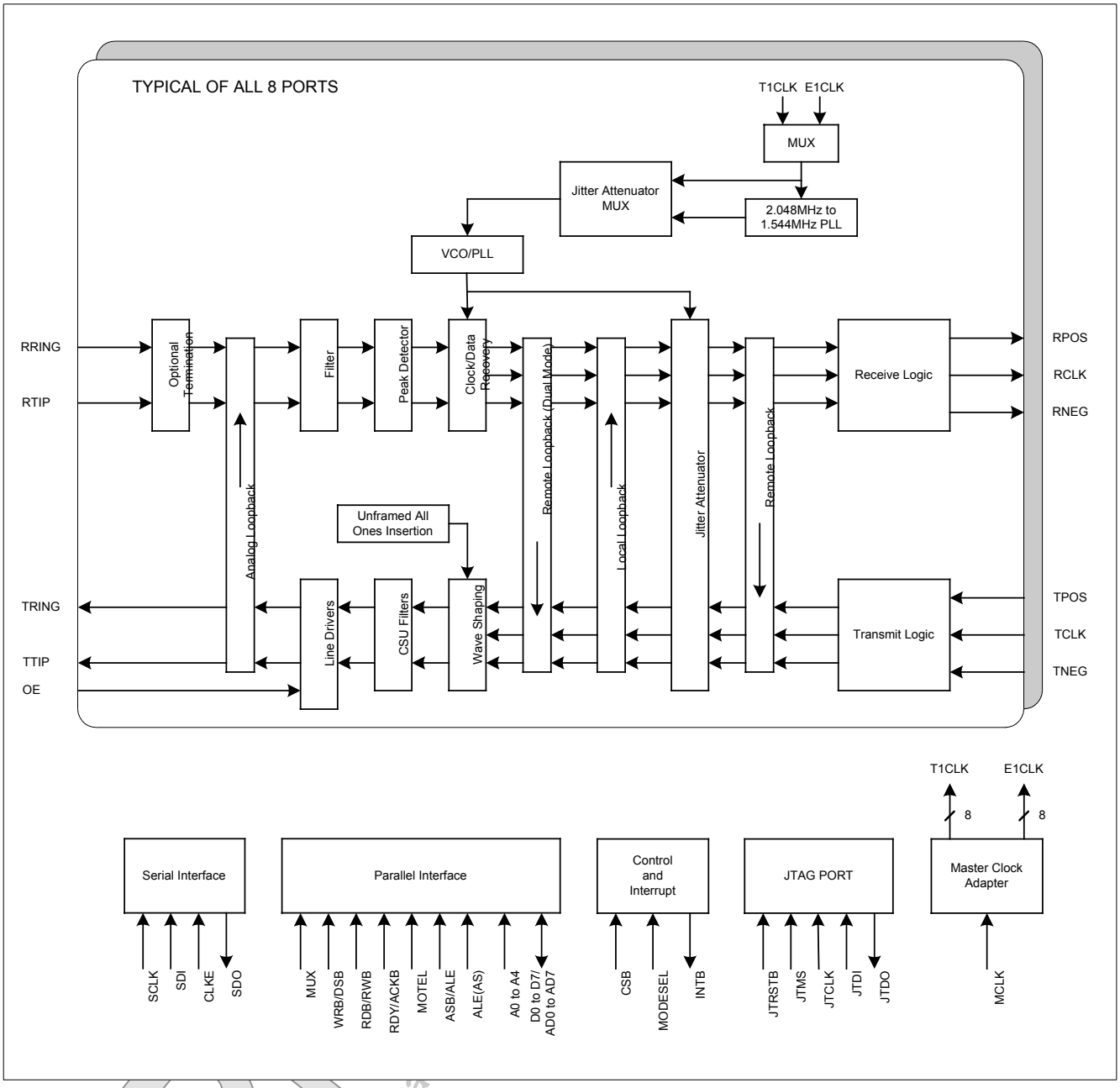

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Figure 1-2 RECEIVE LOGIC DETAIL

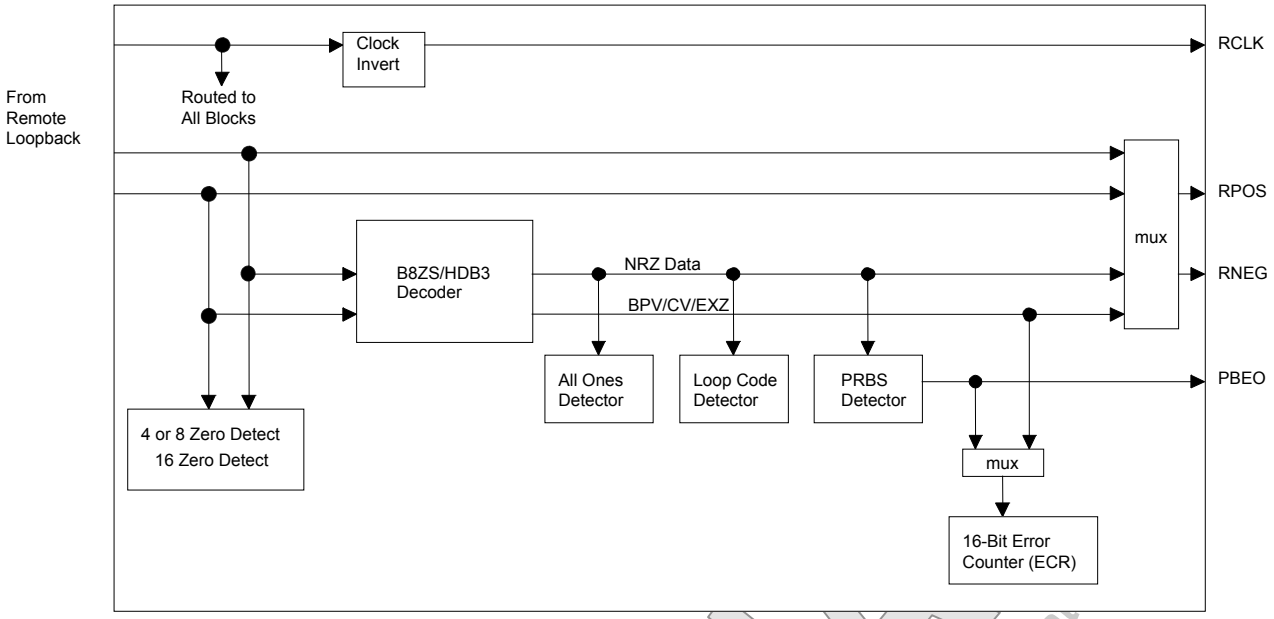
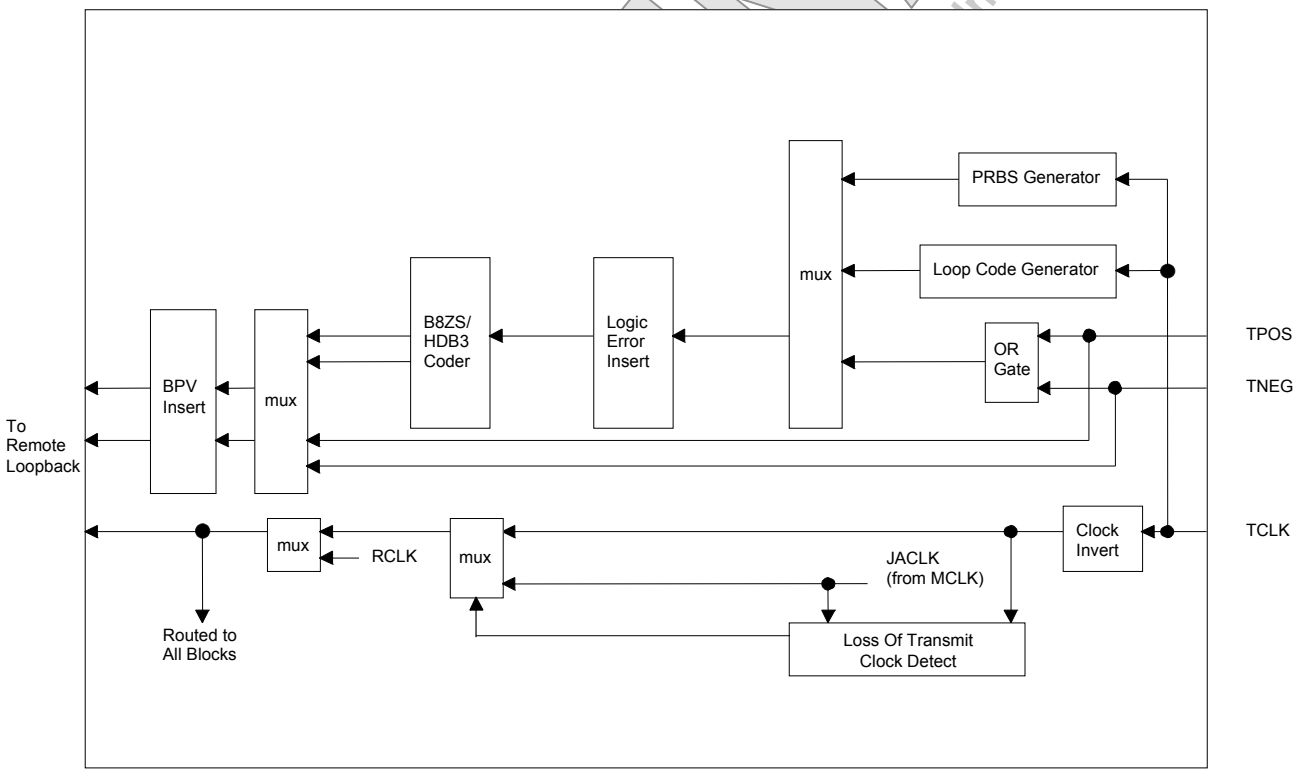


Figure 1-3 TRANSMIT LOGIC DETAIL



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FUNCTIONAL DESCRIPTION

1.1 PORT OPERATION

1.1.1 HARDWARE MODE

The DS26303 supports a standalone hardware configuration mode that allows the user to configure the device through setting levels on the device's pins. This mode allows the configuration of the DS26303 without the use of a microprocessor. Not all of the device features are supported in the hardware mode.

1.1.2 SPI BUS PROTOCOL

SPI is a four wire serial bus for 8- or 16-bit transfers from a master device to a slave. Data transfers are always initiated by the master device, which also generates the clock. The three main signals are Serial Port Clock, Serial Data In, and Serial Data Out. A fourth signal CSB (active low) is used as a chip select to select the slave device that is the intended target of the bus transfer.

1.1.3 PARALLEL PORT OPERATION

The DS26303 provides an 8-bit parallel port used for device configuration and status. The port can operate with either Intel or Motorola bus-timing configurations.

1.1.4 INTERRUPT HANDLING

The DS26303 provides interrupt support for the following events: jitter attenuator limit trip, transmit line open circuit transmit line short circuit and receive loss of signal.

The interrupt functions as follows:

- When status changes on an interruptible event, INTB pin will go low if the event is enabled through the corresponding Interrupt Mask Register. The INTB has to be pulled high externally with a 10K ohm resister for wired-or operation.
- When an interrupt occurs the host processor has to read the interrupt status register to determine the source of the interrupt.
- Subsequently the host processor can read the corresponding status register and this will clear the interrupt status register.
- When there are no pending interrupts the INTB will goes high.

1.2 LIU

The DS26303 is comprised of 8 identical LIU transmit and receive circuits. The DS26303 provides software selectable internal receive and transmit termination for 100 Ω T1 twisted pair, 110 Ω J1 twisted pair, 120 Ω E1 twisted pair and 75 Ω E1 coaxial applications. The DS26303 transmit waveforms meet the corresponding G.703 and T1.102 specification. The receiver LIU can function with a receive signal attenuation of 15 dB.

1.2.1 Transmitter

The transmitter receives NRZ data from the system side interface. The data is encoded with HDB3, B8ZS or AMI. The encoded data passes through a jitter attenuator if it is enabled for the transmit path. A digital sequencer and

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DAC are used to generate transmit waveforms. The transmitter requires a transmit clock of 2.048 Mhz for E1 or 1.544 Mhz for T1J1 operation. The relevant telecommunications specification compliance is shown in Table 1.2-1.

Table 1.2-1 The Telecommunications Specification Compliance for DS26303 Transmitters

Transmitter Function	Telecommunications Compliance
T1 Telecom Pulse Mask Compliance	ANSI T1.403
T1 Telecom Pulse Mask Compliance	ANSI T1.102
Transmit Electrical Characteristics for E1 Transmission and Return Loss Compliance	ITUT G.703.

1.2.1.1 Transmit Line Pulse Shapes

The DS26303 the transmitters can be selected individually to meet the pulse masks for E1 and T1/J1 modes. The transmit pulse can be configured for each LIU on an individual basis. The transmitters can be programmed for internal transmit terminating impedance of 100 ohms for T1, 110 ohms for J1 Mode, 75 or 120 ohms for E1 Mode or no internal termination for E1 or T1 Mode. In this case the user has to provide the line-terminating network. The pulse shapes will be complaint to T1.102 and G.703.

1.2.1.2 Transmit Power down

The transmitters have fast High-Z capability through register settings or pins and can be individually powered down. Note that powering down the transmit LIU results in a High-Z state for the corresponding TTIP and TRING pins.

When transmit all ones is invoked, continuous ones are transmitted using MCLK as the timing reference. Data input at TPOS and TNEG is ignored. Also, transmitting of all ones can be enabled if the corresponding receiver goes into loss of signal state.

1.2.1.3 Driver Fail Monitor

A driver fail circuit monitors the TTIP and TRING pins. It will detect a short circuit or an open circuit condition on the secondary side of the transmit transformer. The drive current will be limited if a short circuit is detected. The driver fail status – open and short circuit can be monitored and if enabled, generate interrupts.

1.2.2 Receiver

The 8 receivers of the DS26303 are all identical. The DS26303 is designed to be fully software-selectable for E1 and T1/J1 without the need to change any external resistors for the receive-side. The output of the internal termination circuitry is fed into an equalizer and subsequently to a peak detector. The receiver is capable of recovering signals with up to 15 dB worth of attenuation.

1.2.2.1 Loss of Signal

The DS26303 uses both the digital and analog loss detection method in compliance with the latest T1.231 for T1J1 and ITU G.775 or ETSI 300 233 for E1 mode of operation.

Loss of Signal (LOS) is detected if the receiver level falls bellow a threshold analog voltage for certain duration of time. Alternatively this can be termed as having received “zeros” for certain duration. The signal level and timing duration are defined in accordance with the T1.231 or G.775 or ETSI 300 233 specifications. The loss detection thresholds are based on cable loss of 18 dB for T1, J1 and E1 Mode.

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The loss state is exited when the receiver detects a certain number of ones density at a higher signal level than the loss detection level. The loss detection signal level and loss reset signal level are defined with a hysteresis to prevent the receiver from bouncing between “LOS” and “no LOS” states.

The following table outlines the specifications governing the loss function:

Table 1.2-2 Loss criteria T1.231, G.775 and ETSI 300 233 specifications

	Standard		
	T1.231	**ITU G.775**	**ETSI 300 233**
Loss Detection Criteria	No pulses are detected for 175 +/- 75 bits.	No pulses are detected for duration of 10 to 255 bit periods.	No pulses are detected for a duration of 2048 bit periods or 1 msec
Loss Reset Criteria	Loss is terminated if a duration of 12.5% ones are detected over duration of 175 +/- 75 bits. Loss is not terminated if 8 consecutive zeros are found if B8ZS encoding is used. If B8ZS is not used loss is not terminated if 100 consecutive pulses are zero.	The incoming signal has transitions for duration of 10 to 255 bit periods.	Loss reset criteria is not defined.

1.2.2.2 ANSI T1.231 for T1 and J1 Modes

Loss is detected if the received signal level is less than -18 dB for duration of 192-bit periods. LOS is reset if the all of the following criteria are met:

- 24 or more ones are detected in 192-bit period with a signal level greater than -15 dB measured at RTIP and RRING.
- During the 192 bits less than 100 consecutive zeros are detected.

1.2.2.3 ITU G.775 for E1 Modes

LOS is detected if the received signal level is less than -18 dB for a continuous duration of 192 bit periods. LOS is reset if the receive signal level is greater than -15 dB for a duration of 192 bit periods.

1.2.2.4 ETSI 200 233 for E1 Modes

LOS is detected if the received signal level is less than -18 dB for a continuous duration of 2048 (1 msec) bit periods. LOS is reset if the receive signal level is greater than -15 dB for a duration of 192-bit periods.

1.3 Jitter Attenuator

The DS26303 contains jitter attenuators that can be set to depths of either 32- or 128-bits. The 128-bit mode is used in applications where large excursions of wander are expected. The 32-bit mode is used in delay sensitive applications. The jitter attenuator can be placed in either the receive path or the transmit path or disabled.

In order for the jitter attenuator to operate properly, a 2.048 MHz or multiple thereof or 1.544 MHz clock or multiple thereof must be applied at MCLK. ITU specification G.703 requires an accuracy of +/-50 ppm for both T1J1 and E1 Applications. TR62411 and ANSI specs require an accuracy of +/- 32 ppm for T1J1 interfaces. Circuitry adjusts either the recovered clock from the clock/data recovery block or the clock applied at the TCLK pin to create a

smooth jitter free clock, which is used to clock data out of the jitter attenuator FIFO. It is acceptable to provide a gapped/bursty clock at the TCLK pin if the jitter attenuator is placed on the transmit side. If the incoming jitter exceeds either 120 UIpp (buffer depth is 128-bits) or 28 UIpp (buffer depth is 32-bits), then the DS26303 will set the Jitter Attenuator Limit Trip (JALTS) bit in the LIU Real Status Register when the FIFO is 8 bits from underflow or overflow. The FIFO pointer will be 8 bits or 120 bits. In T1J1 mode the Jitter Attenautor corner frequency is 3.75 Hz and in E1 mode it is 0.6 Hz.

Table 1.3-3 Jitter Attenuator Standards Compliance

ITUT I.431, G.703, G.736, G.823,
ETSI 300011, TBR 12/12
AT&T TR62411, TR43802
TR-TSY 009, TR-TSY 253, TR-TSY 499

1.4 LIU Loopbacks

The DS26303 provides four LIU loop backs for diagnostic purposes; Analog Loopback, Digital Loopback, Remote Loopback and Dual Loop back.

1.4.1 Analog Loop back

The analog output of the transmitter TTIP and TRING is looped back to RTIP and RRING of the receiver. Data at RTIP and RRING is ignored in analog loop back. This is shown in Figure 1.4-1.

1.4.2 Local Loop back

The transmit data TPOS and TNEG and TCLK will be looped back to output on RCLK, RPOS and RNEG. Data input at TPOS and TNEG will be encoded and output on TTIP and TRING. Signals at RTIP and RRING will be ignored. This loopback is conceptually shown in Figure 1.4-1.

1.4.3 Remote Loop back

The inputs decoded from the RRING and RTIP are looped back to the transmitter. The inputs from the transmit side TPOS and TNEG and TCLK are ignored during a remote loopback. This loopback is conceptually shown in Figure 1.4-1.

1.4.4 Dual Loop back

The inputs decoded from the RRING and RTIP are looped back to the transmitter. The inputs from TPOS, TNEG and TCLK are looped back to the receiver with the optional jitter attenuator. This loop back is conceptually shown in Figure 1.4-1.

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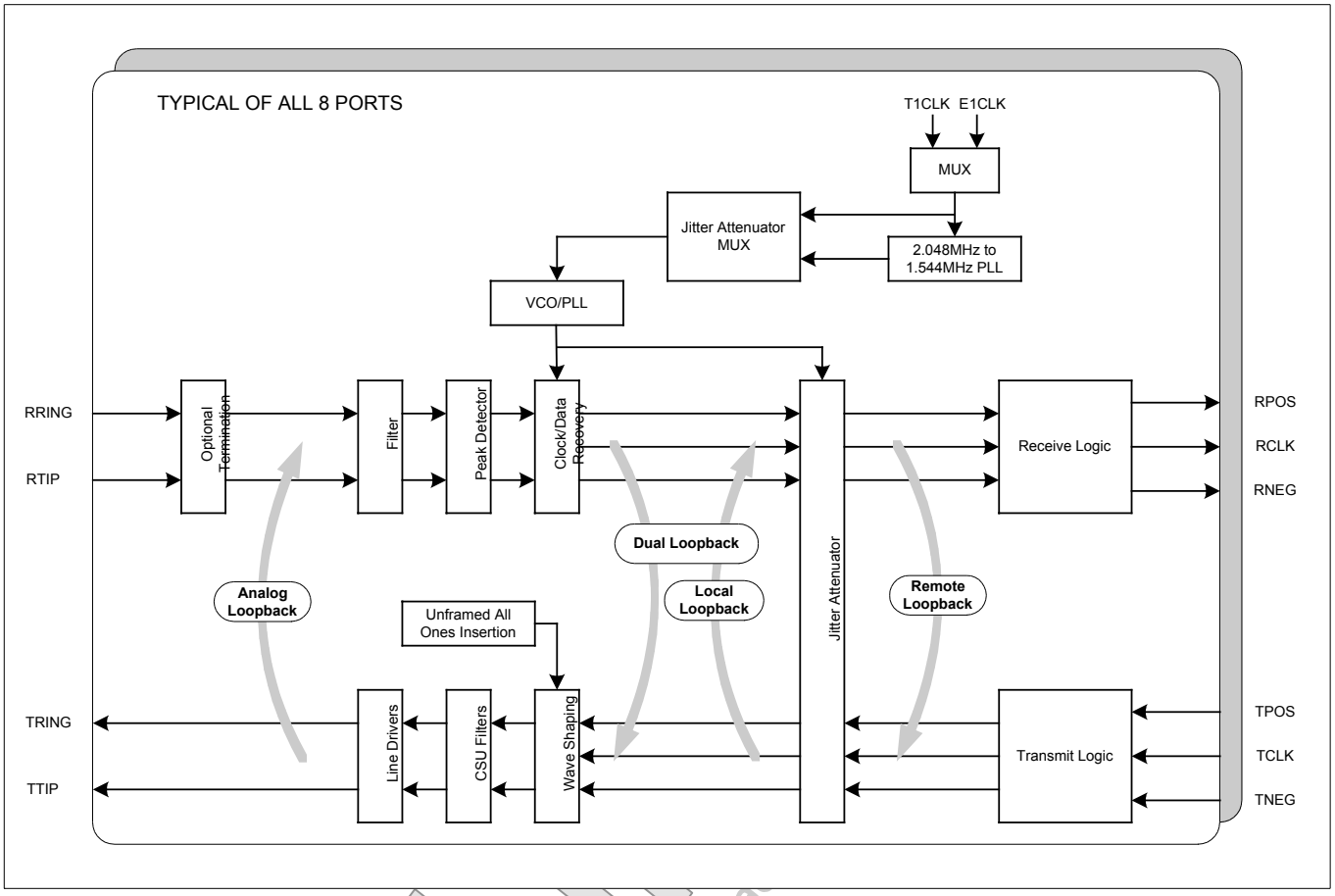
Figure 1.4-1 Loop Back Paths



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